

Wafer Level Packaging

The Challenge

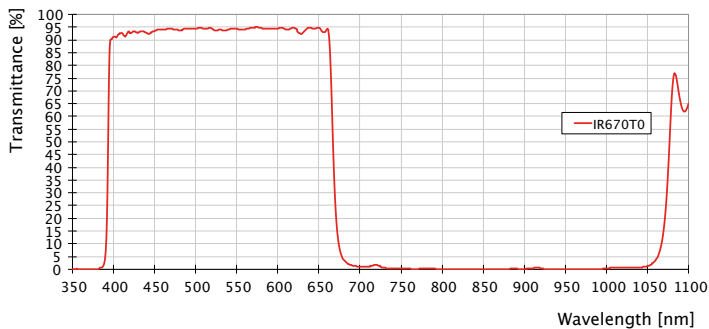
Materion Barr Precision Optics & Thin Film Coatings wafer level packaging is leading edge technology for high volume advanced optical packaging. The glass wafer is merged with the silicon wafer before dicing. Some applications will require a spacer between the two wafers. We provide high quality glass wafers with low defect optical coatings, or if required, with chrome apertures for light beam shaping.

Benefits

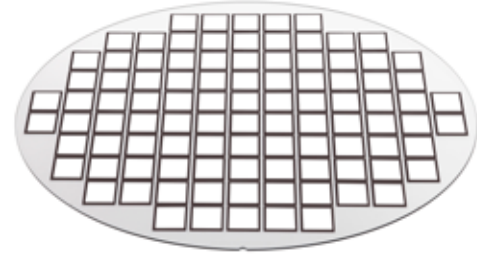
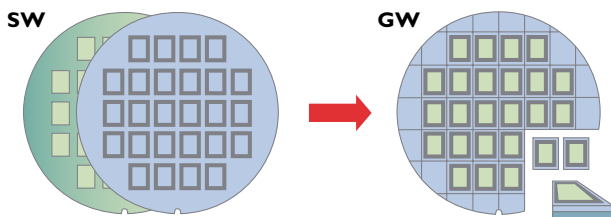
- High cleanliness at assembly step
- High yields due to clean work pieces
- Reduced handling efforts
- Lower cost due to parallel assembly step on devices
- Enables further miniaturization

Applications/Technical Data

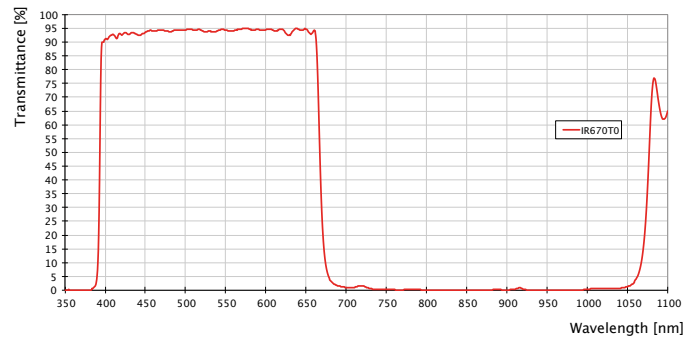
IR Cut Filters on WLP



- **Applications** CMOS Packaging
- **Size of wafer** 200 mm round, 0.3/0.4 mm thick
- **Typical glass type** Schott D263T
- **Defect level** No defects > 50 μm

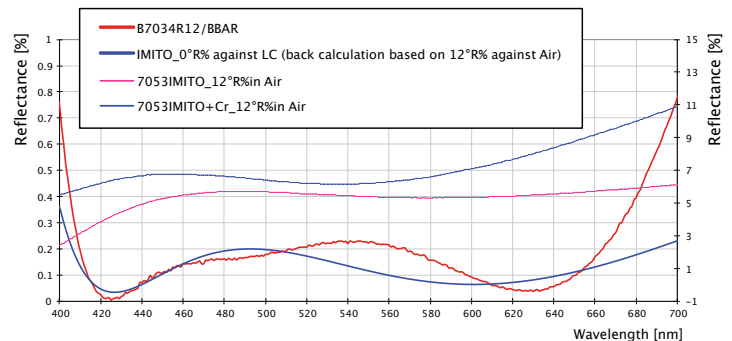


Anti Reflex Coatings on WLP



- **Applications** MEMS/CMOS Packaging
- **Size of wafer** 200 mm round, .07/0.4/0.3mm thick
- **Typical glass type** Borofloat, Eagle XG, AF32
- **Defect level** No defects > 20 μm

Index Matched ITO on WLP



- **Applications** LCOS Microdisplays Packaging
- **Size of wafer** 200 mm round, 0.7/0.4/0.3mm thick
- **Typical glass type** AF32, Eagle XG
- **Defect level** No defects >20 μm on ITO side

Schematic Wafer Level Packaging: Entire semiconductor wafer (SW) with array of sensors is covered by a cover glass wafer (GW) – see left side. Combined wafers are cut into pieces (right side).

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