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PVD Principles Key To The Microelectronics Industry

The fundamentals of PVD processes are deeply embedded in the fabrication of microelectronic devices.

February 2021 | Samuel Pellicori & David Sanchez

Introduction

In this technical article, we emphasize materials, processes, and applications relative to the world of microelectronics. As LiDT (Laser induced Damage Threshold) mitigation technology challenges materials and deposition technologies to meet performance requirements for laser optics, the fabrication of integrated circuits in the microelectronics industry requires optimization at each step, from wafer to device. Layer by layer, lithographic patterning, metal and dielectric coating, selective chemical and plasma etching, and process control are employed to minimize cost and maximize performance of the device.

We will address fundamentals of physical vapor deposition (PVD) processes that are deeply embedded in the fabrication of microelectronic devices. As transistors and gates shrink, the quality of the metal, insulator or semiconductor, in addition to their processing, impact the performance of the device. Device feature size is dependent on the wavelength of the pattern projected through the photolithographic mask. To achieve the highest resolution and smallest physical features, transmissive excimer DUV lithography and reflective EUV lithography are employed to meet the needs of the industry.

Choice of PVD Deposition Process

PVD processes are used in microelectronic device fabrication and as seed layers for plating. PVD includes thermal evaporation by e-beam or resistance-heated evaporation and sputter deposition.

Advantages of Employing PVD Processes

PVD coatings are hard, more amorphous and homogeneous, and have high temperature durability, good impact strength, and excellent abrasion resistance. Therefore, protective topcoats are rarely needed on high-performance devices.

- PVD processes utilize virtually any type of inorganic and some organic coating materials on an equally diverse group of substrates and surfaces across a range of processing temperatures.
- Sputtered seed layers work with electroplating and are compatible with many types of photoresist and removal techniques.
- More than one technique can be used to deposit a given film allowing them to be combined in cluster tools or stand alone as a batch process.

Disadvantages of Employing PVD Processes

Line-of-sight transfer is typical of most PVD coating techniques, however there are methods that allow full coverage of complex geometries.

- Some PVD technologies consume a large amount of power to sustain, may require very high vacuum, and require frequent shield or foil changes due to buildup.
- Reactive gas delivery can require sophisticated control and distribution, individual cooling schemes for sources, and the chamber to protect the substrates or assure proper film composition or grain size can be a challenge.

Sputter Deposition

As we have discussed in past articles, sputter deposition offers many advances compared to other PVD methods [1, 2, 3]. A wider variety of metals and dielectrics can be sputter deposited at lower substrate temperatures. The varieties of sputter

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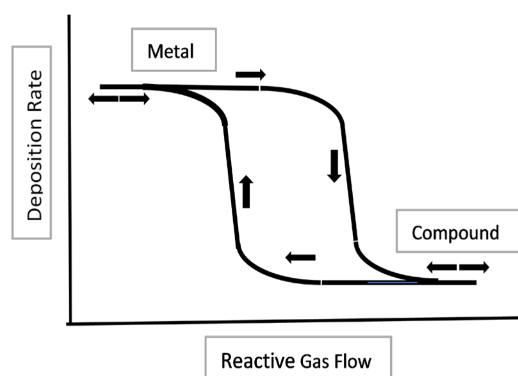
deposition techniques include DC, AC (RF), reactive, and magnetron. These processes involve energetic plasmas operating at pressures >1 mbar. Ion beam sputtering (IBS) operates at <10-4 mbar [3]. Magnetron sputtering (MS) can be configured for DC, AC, RF or reactive deposition, and is used in the microelectronics industry. Magnetron sputtering (MS) enables deposition of metal conductors and dielectric insulators uniformly over large wafer areas with low defects and minimal thermal distortion. Powerful magnetic fields yield higher current densities during MS, thus enabling deposition rates to be faster. Metal targets are used in reactive AC or pulsed-power DC MS (PDCMS) to produce dielectric or metal layers depending on the presence or absence of reactive gases such as oxygen and nitrogen. Two advantages of reactive MS of metal targets includes better stoichiometric purity and fewer structural defects.

Mastery of the sputtering hysteresis is a critical advantage of the technique. Some of the most common and important reactive processes for optics and integrated circuits are those of Silicon (Si), Titanium (Ti), Tantalum (Ta), and Aluminum (Al) metal, Oxide and Nitride and Hafnium (Hf) Oxide. An ion plasma consisting of Ar+ ions does the work of physically sputtering atoms from the cathode (target) surface by the momentum transfer of kinetic energy. With the addition of reacting gasses in the reactive sputtering process compound, compositions can be sputter deposited. In the reactive mode, MS deposits layers of oxide- or nitride-compounds with high stoichiometric purity and high dielectric properties. Since the layers in a device structure are thin, high dielectric constants are required in the insulating layers that compose circuits. In the reactive mode, cyclic behavior between a metal surface and an oxide (nitride) layer on the target (cathode) is related to the deposition rate vs gas flow rate at constant discharge current and follows a hysteresis behavior shown in Figure 1.

Figure 1



The deposition rate of a compound generated from reactive sputtering of the metal target (cathode) follows a hysteresis curve. At constant current density, deposition of either metal or metal compounds depends on reactive gas flow rate.

The deposition of the desired dielectric composition occurs on a downward trending section of the cycle. Here the system needs stable control of parameters to maintain consistent compound stoichiometry. During the sputtering of a metal target in the reactive mode, reaction with the target surface inevitably occurs as an oxide or nitride surface is generated on the target. Deeper into this poisoning of the target, the charge can build up on an insulating layer and consequent arcing with particle ejection can degrade or destroy the deposited film properties. The rate of growth of the insulating coating is determined by the power density at the target and the partial pressure of reactive gas pressure.

For the deposition of dielectrics, a critical balance must be maintained between reactive gas consumption that is present at the target surface and in compound formation on the substrate. An operating point on the curve is maintained through feedback control of pressure and power. Often, a plasma emission spectrometer is employed for that purpose. Great care is also taken during process development to minimize film stress.

During target poisoning, Insulating oxide (nitride) layers can grow on the target surface and cause a severe decrease in deposition rate as well as arcing. To prevent this occurrence, the polarity between cathode (target) and anode can be reversed as in the AC or RF mode. The pulsed DC magnetron sputter (PDCMS) mode operates on the same principle using voltage pulsing in the kilohertz frequency range. Deposition of charge by ions occurs during the on segment of the cycle, electrons dissipate the charge during the off segment. The frequency that prevents micro-arcing is chosen as a parameter appropriate for the material being sputtered. Trends of microarcs are often tracked to reduce hard arcs which cause catastrophic damage to the coating. Because of the low substrate temperatures used, sputtering is an ideal method to deposit contact metals for thin-film transistors and low stress compounds.

Semiconductor Device Fabrication

Semiconductor devices such as photo sensors, light emitters and solar cells are layer devices constructed sequentially with light to moderate use of lithography. The dimensions of sensors used in cameras, automotive and aeronautics displays, and consumer products including LED and OLED television screens, smart phones, virtual reality, and video gaming are required to be progressively smaller to enable higher spatial resolution and greater response speeds to be advanced. CPUs, memory chips, and power electronics require heavy use of lithography as each layer is interconnected and may require modification beyond the coating, including ion implantation and selective etching.

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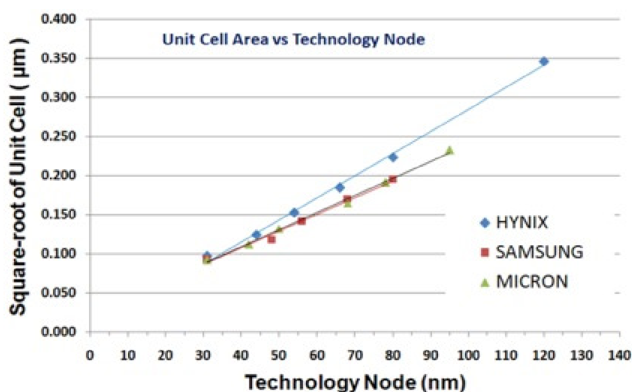
In optics, the minimum feature resolution is determined by the wavelength of the source and f/no. (or the numerical aperture) of the optics according to the optical diffraction limit, D = 2.44 wvl x f/no. or D = 2.44 wvl x 1/ 2n (N.A.), where N.A. = numerical aperture and n is the refractive index of the medium between the last imaging optic and photoresist on the wafer to be patterned. In the quest to produce higher device densities, photolithography has used shorter wavelength light sources including mercury vapor lamp (365nm), and more recently KrF (248nm) and ArF (193nm) excimer lasers. The wavelength of the UV source is linked directly to the minimum feature size possible and the ability of the system to image features with precision. Imaging in water instead of air is known as immersion lithography. The index of water at 193 nm is 1.44 vs that of air at 1.0. That larger index permits features as small as 35 nm to be imaged with the 193 nm laser.

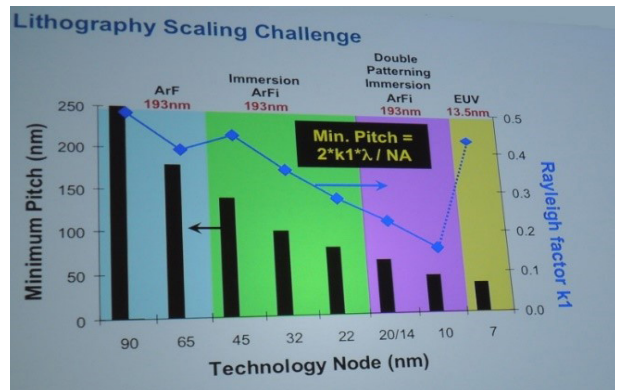
The migration to 193nm DUV laser light as the most common source for both dry and immersion lithography and drove refinement of the photocatalytic polymer resists as well. The new photoresists enable more efficient removal and reduce defects over what could be a one week to a one month-long fabrication of devices. In moving away from classical "technology nodes" toward smaller transistors or shorter gates, profound technological refinements continue to push innovation and investment in the Front End of Line (FEOL) or first metal layer on the silicon substrate. The race to image features smaller than 60nm in length continues to drive DUV multi-exposure and EUV light source technologies. High power CO2 laser discharge is used to excite Sn plasma at a wavelength of 13.5 nm. Molybdenum and Silicon Multi-layer UV mirrors are used for collection, condensing and imaging mirrors. A photolithographically-produced reflecting mask images the smallest features to be exposed for subsequent processing into todays most sophisticated memory and CPU architectures.

Figure 2



The trend in reducing feature size and therefore device density expressed as technology node. Source: "Hynix DRAM layout, process integration adapt to change", by Arabinda Das

Figure 3



Scaling of device dimensions related to fabrication process.
Source: "IBM outlines fab future beyond FinFETs", by Rick Merritt

Conclusion

This article is a brief review of sputtering technology and challenges to lithography, it also shows where PVD remains an essential technology in the microelectronics and semiconductor industries. Developments in EUV photolithography have enabled smaller features to be resolved with the results of greater feature density, greater processing speeds and higher memory capacity. Lithography enables specialization at each layer as the device rises from the silicon substrate. Reactive sputtering compliments a high-quality metal mode with a customizable oxide, nitride or oxynitride compound formation with few vacancies at a moderate or low substrate temperature. As a contact, a diffusion barrier or an insulator sputtering can optimize metals consumption and suppresses unstable states throughout the iterative process of making complex devices.

In future articles, we will discuss how those layers are employed by different applications. It is difficult to extrapolate the limits of the technology, and the connection between classical optical coatings, laser light sources and the future of computing.

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